Remarks

Reconsideration of this application is requested. By this response to the Office Action, claims 1-4 and 18 were amended, and claims 5-17 and 19-48 were canceled. A listing of claims and the actions taken is included in this amendment. Claims 1-4 and 18 remain in the application.

Objections to claims 10, 27, 33-39, 42-43 and 48

The Office Action objects to claim language and duplicate claims. Claims 10, 27, 33-39, 42-43 and 48 have been canceled by this amendment.

Response to the 35 U.S.C. §112 Rejection

The Office Action rejects claims 7, 9-10, 14, 28-29, 32, 42 and 46 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

By this amendment claims 7, 9-10, 14, 28-29, 32, 42 and 46 have been canceled and the rejection of these claims is now moot.

Response to the 35 U.S.C. §102(b) Rejection

The Office Action rejected claims 1-48 under 35 U.S.C. §102(b) as being anticipated by D'Luna et al. (U.S. Patent No. 5,311,459). By this amendment claims 1-4 and 18 remain in this application.

Claims 1-4

Applicant's claim 1 recites, among other things, first and second multiplexers; and a multiplication block including a first multiplication unit and an adder unit selectively connectable in different configurations, a first configuration coupling first and second inputs of the first multiplication unit to outputs of the first and second multiplexers to receive first and second operands, and a second configuration coupling first and second inputs of the adder unit respectively to the outputs of the first and second multiplexers to receive the first and second operands.

Support for Applicant's amended claim language can be found in the figures in at least FIG. 3A where first and second inputs of the first multiplication unit (unit mult0) are coupled to outputs of the first and second multiplexers to receive first and second operands (inp0 and inp1); and FIG. 3B where first and second inputs of the adder unit (add0) are respectively to the outputs of the first and second multiplexers to receive the first and second operands (inp0 and inp1).

D'Luna et al. teach a computation block for performing digital signal computations to provide different functions under mode selection control. FIGs. 1-5 show a multiplier coupled to receive a first coefficient from a switch element and a second coefficient from a multiplexer. D'Luna et al. teach an adder unit that provides a sum-of-products. Thus, the adder unit taught by D'Luna et al. only has inputs connected to the outputs of the multipliers.

This configuration to provide the sum-of-products taught by D'Luna et al. is in contrast to Applicant's amended claim 1 that provides two configurations. Namely, a first configuration where a multiplication unit receives operands from multiplexers and a second configuration where an adder unit receives the operands from the multiplexers. Since this feature is not taught or suggested by the replied upon reference, Applicant's claim 1 is not anticipated by D'Luna et al. and the rejection should be removed.

Claims 2-4 depend, either directly or indirectly, from base claim 1 and are believed allowable over the art of record for at least the same reasons as claim 1.

Claim 18

Applicant's claim 18 recites, among other things, a first configuration instruction to the multiplication block configures the multiplication unit to receive first and second operands from the first and second multiplexers and provide a product of the operands at an output, and a second configuration instruction configures the first and second adder units to receive the first and second operands from the first and second multiplexers and provide a summed value of the operands.

Again, D'Luna et al. only teach an adder unit that provides a sum-of-products which fixes the connection of the adder to outputs of the multipliers. D'Luna et al. do not teach Applicant's claimed feature that a second configuration instruction configures the first and second adder units to receive the first and second operands from the first

and second multiplexers. Accordingly, Applicant believes that claim 18 is patentable over the relied upon art of record and the rejection of claim 18 under 35 U.S.C. §112, second paragraph, should be removed.

Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed August 16, 2004, and reconsideration of the objections and rejections is requested. It is submitted that claims 1-4 and 18 are now in condition for allowance. Allowance of these claims is earnestly solicited.

Applicants herewith petition the Director of the United States Patent and Trademark Office to extend the time for response to the Office Action dated August 16, 2004, for 2 months. Please charge Deposit Account #50-0221 in the amount of $430.00 for a two month extension. Should it be determined that an additional fee is due under 37 CFR §1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities that can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 715-5388 is respectfully solicited.

Respectfully submitted,
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